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IN THE U.S. PATENT AND TRADEMARK OFFICE

Appl. No.:	10/691,252
Applicant:	Michael Buchmann
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Examiner:	Bao Q. Vu
Docket No.:	890A.0001.U1(US)
Customer No.	29683
Title:	Voltage Multiplier with Charge Recovery

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S APPEAL BRIEF

Sir:

Commensurate with the Notice of Appeal filed on 5 September 2006, Applicant/Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences (hereinafter, the Board) under 37 C.F.R. §41.31. The $500 appeal brief fee set forth in 37 C.F.R. §41.20(b)(1) was previously paid on 27 December 2005. The Examiner reopened prosecution after the Appeal Brief was filed. Consequently, no new appeal brief fee should be due. However, should the undersigned representative be mistaken, please debit Deposit Account No. 50-1924 as appropriate.

This Appeal Brief is filed within one month from reception of a Notice of Panel Decision from Pre-Appeal Brief Review. The undersigned representative believes that no late fee is due. However, should the undersigned attorney be mistaken, please consider

this a petition for an extension of time under 37 C.F.R. §1.136(a) or (b) that may be required to avoid dismissal of this appeal, and debit Deposit Account No. 50-1924 as appropriate.

(1) REAL PARTY IN INTEREST

The real party in interest (RPI) is Nokia Corporation of Espoo, Finland, as indicated in an assignment of the U.S. application recorded on October 22, 2003 at reel 014638 and frame 0238.

(2) RELATED APPEALS AND INTERFERENCES

There are no other pending appeals or interferences of which the undersigned representative and assignee/RPI is aware that will directly affect, be directly affected by or have a bearing on the Board's decision in this appeal.

(3) STATUS OF CLAIMS

Claims 1-8 are pending in this appeal and stand finally rejected. Claims 1-8 are reproduced in an Appendix accompanying this Brief as those claims stood finally rejected by a final Office Action dated 6 July 2006.

(4) STATUS OF AMENDMENTS

No amendments are pending. All amendments have been previously entered.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Reference may be had to FIGS. 1, 10a, 10b, and 11 for this Summary. Independent claim 1 is directed to a capacitive voltage multiplier (FIG. 1, FIG. 11) for generating voltage pulses that are higher than the supply voltage (e.g., the voltage on input 31; see page 7, lines 20-23). The multiplier (FIG. 1, FIG. 11) includes a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier. The

switching capacitor circuit (21) is provided with capacitors (e.g., capacitors 11, 12, 13 of FIG. 11) and is further provided with switches (e.g., switches 1-8 of FIG. 11) for charging the capacitors (e.g., capacitors 11, 12, 13 in FIG. 11) in parallel and discharging them in series in order to deliver a high voltage pulse. See also FIGS. 10a and 10b regarding operating switches S1-S12 in order to charge capacitors C1 through C4 in parallel and discharge the capacitors C1 through C4 in series. The multiplier (FIG. 1, FIG. 11) further includes a diode chain circuit (22) coupled between the input (31) and output (32) terminals of the multiplier (FIG. 1, FIG. 11), said diode chain circuit (22) includes a diode-chain (e.g., diodes 41, 42, 43 and 102 of FIG. 11). The diode chain circuit (22) includes pumping capacitors (e.g., capacitors 51, 52, and 53 of FIG. 11) for delivering high voltage current. See also the description from page 6, line 6 to page 8, line 3.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

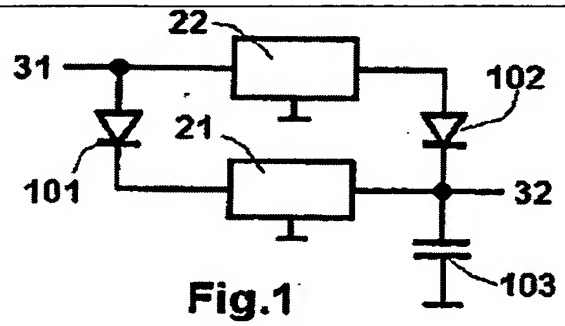
The only ground for rejection presented for review by the Board is whether claims 1-8 are unpatentable as being obvious under 35 U.S.C. §103(a) by Kazerounian et al., U.S. Patent No. 5,006,974 (hereinafter, Kazerounian) in view of Yu, U.S. Patent No. 5,0006,974 (hereinafter, Yu).

(7) ARGUMENT

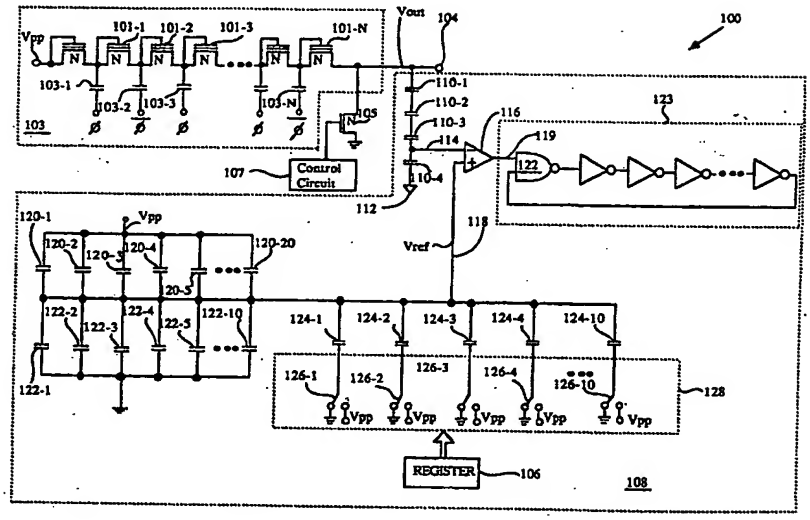
Claims 1-8 stand rejected as being obvious under 35 U.S.C. §103(a) by Kazerounian in view of Yu. This is the sole ground for rejection. Claim 1 is the sole independent claim.

CLAIM 1

A portion of independent claim 1 is shown on the left side of the following table. On the right side, a portion of FIG. 1 of the present application is shown for ease of reference. FIG. 11 shows examples of elements 21 and 22 in greater detail.

Capacitive voltage multiplier ..., wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse, characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier, said diode chain circuit (22) comprising a diode-chain and pumping capacitors for delivering high voltage current.	 Fig.1

The Examiner asserts that "Kazerounian discloses a capacitive multiplier circuit having a diode chain (103) and a charge pump circuitry (128) that [is] connected between the input and output of the multiplier circuit (100)." See final Office Action dated 6 July 2006. The Examiner appears to assert that block 103 meets the subject matter of "a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier" in independent claim 1. In the outstanding Office Action, the Examiner cites and displays FIG. 2 from Kazerounian, reproduced below:



It is noted that the Examiner combines Kazerounian with a cited portion of Yu. However, before proceeding further with a discussion of the Examiner's argument and a refutation thereof, it is helpful to review Kazerounian. The following description in the instant paragraph is from Kazerounian, col. 8, lines 9-38. The capacitors 110-1 through 110-4 act as a voltage divider. Comparator 116 compares V_{OUT} and V_{REF} and produces a signal 119 for input into ring oscillator circuit 124 (incorrectly marked as 123 in FIG. 2). When V_{OUT} is not equal to V_{REF}, ring oscillator circuit 124 generates "clock signals ϕ and $\overline{\phi}$, and thus voltage multiplier 100 will increase voltage V_{OUT} at lead 104. However, as soon as voltage $V_{OUT}/4$ is greater than or equal to voltage V_{REF} (note that there is some hysteresis; see Kazerounian at col. 9, line 62 to col. 10, line 13), the signal at output lead 119 goes low, ring oscillator 124 stops oscillating and voltage multiplier 100 stops increasing voltage V_{OUT}. Thus, the EEPROM of the present invention includes a voltage regulator which permits voltage V_{OUT} to be accurately controlled." Kazerounian, col. 8, lines 30-38. The clock signals ϕ and $\overline{\phi}$ are inputs into block 103 (note that capacitors 103-1 to 103-N are also marked as "103"). The output of voltage multiplier 100 is the output lead 104, which carries V_{OUT}. The "input" to block 103 is V_{PP}.

Furthermore, the circuitry in Kazerounian is specifically designed so that one can select the ***lowest*** Vout 104 that erases an EEPROM. The selection is performed using the register 106 and a particular process. See the text from col. 8, line 52 to col. 9, line 38 of Kazerounian. In particular, Kazerounian states the following:

> This process continues until a voltage is selected which is sufficient for erasing the EEPROM. Thereafter, the contents of nonvolatile register 106 are no longer changed, and the EEPROM is erased with the selected voltage. By limiting voltage V_{OUT} to a voltage large enough to erase the EEPROM but not greater, the transistors exposed to voltage V_{OUT} will not be excessively stressed.

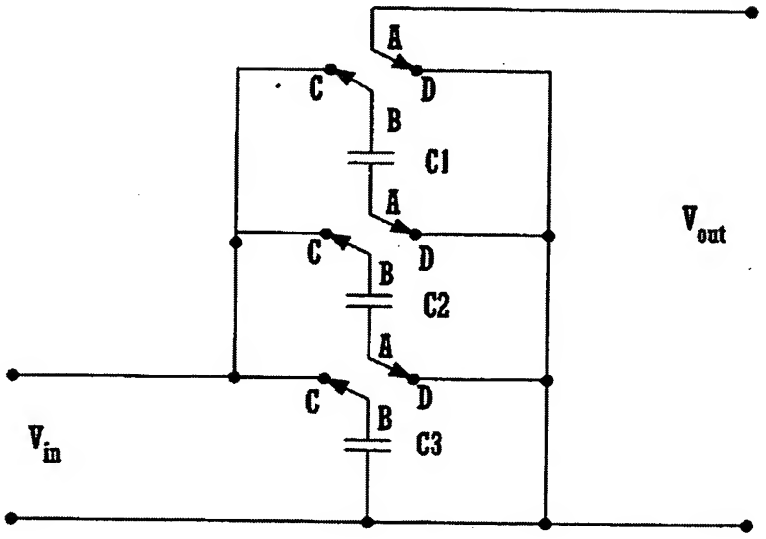
Kazerounian, col. 9, lines 31-38.

Based on the cited sections of Kazerounian, Applicant reads Kazerounian as providing a voltage multiplier circuit 100 that allows selection of a reference voltage, V_{REF}, based on contents of a register. Kazerounian discloses a voltage multiplier circuit 100 that is ***carefully designed*** to allow selection of the lowest V_{OUT} that will allow an EEPROM to be erased.

Into this carefully designed system, the Examiner asserts that a multiplier/charge pump having capacitors charged in parallel and discharged in series should be added. The Examiner cites Yu, col. 1, lines 18-22 for disclosure of a "switching capacitor circuit". The cited section of Yu states the following:

> Switching capacitor is one of the original concepts for the energy conversion. It is available in very limited application such as the energy source for high voltage discharge by connecting an array of capacitors in parallel configuration for charging and in series configuration for discharging.

Yu, col. 1, lines 18-22. The Examiner does not appear to cite any other portion of Yu. However, for reference, here is FIG. 2 of Yu:

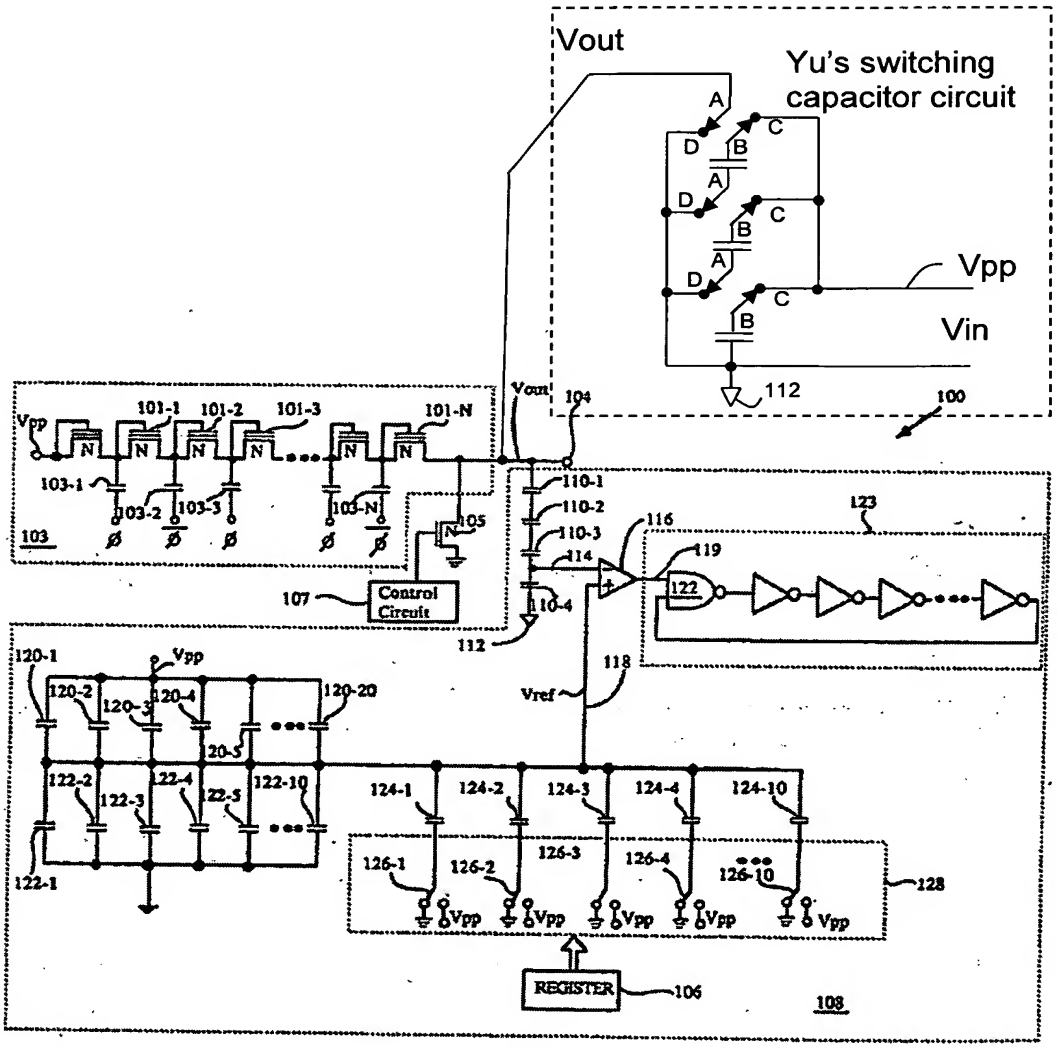


Yu describes this figure as follows:

> FIG. 2 also shows the step-up configuration in similar way as described in FIG. 1. The only difference is that the capacitors C1, C2, and C2 are connected in parallel configuration during charging and in series configuration during discharging. The output voltage Vout is about three times of the input voltage Vin in this case.

Yu, col. 2, lines 60-65. It is believed that capacitors C1-C3 are connected in parallel and charged when the switcher connects B→C and A→D. The capacitors C1-C2 are connected in series and discharged when the switcher connects A→B. See Yu, col. 2, lines 45-59. In particular, see FIG. 3 of Yu, which describes a switcher, and in which it can be seen that when V_g is high, A is connected to B, whereas when V_g is low, A is connected to C and B is connected to D.

In order for the switching capacitor circuit (e.g., shown in FIG. 2) of Yu to be added into the invention in Kazerounian and meet the subject matter of independent claim 1, the following would have to occur (as illustrated by a modified version of FIG. 2 of Kazerounian):



This modified figure of Kazerounian shows the "switching capacitor circuit" in FIG. 2 of Yu (called "Yu's switching capacitor circuit") combined with the voltage multiplier 100 of FIG. 2 of Kazerounian. The circuit shown in this figure is called the "combination circuit" herein. Note that, in the above figure, the switching capacitor circuit of FIG. 2 of Yu has been reversed so that Vin is on the right and Vout is on the left. This combination circuit meets the Examiner's assertions, as the Examiner appears to assert that element "103" meets the subject matter of "diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier". Assuming, *arguendo*, the Examiner's

assertion is true, V_{PP} is the input of block 103 and V_{OUT} (e.g., output lead 104; called V_{OUT} 104 below) is the output for both block 103 and voltage multiplier circuit 100. Then, in order for Yu's switching capacitor circuit to meet the subject matter of "a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier" in independent claim 1, the switching capacitor circuit would be placed between V_{PP} and V_{OUT}, as shown above in the modified FIG. 2 of Kazerounian.

For at least the following reasons, the combination of Kazerounian and Yu is improper and the requirements of a *prima facie* case of obviousness are not met:

First, the circuitry of Kazerounian already produces a high output voltage on V_{OUT} 104 (see FIG. 2 of Kazerounian). There is no benefit to adding yet another circuit (i.e., from Yu) for producing a high voltage on V_{OUT} 104 of Kazerounian. Furthermore, the circuitry of Kazerounian already provides a range of output voltages. It is believed (as described in more detail below) that adding Yu's switching capacitor circuit to the voltage multiplier 100 would lower that range, which would be detrimental.

Second, combining two circuits (block 103 in Kazerounian and the circuit described at col. 1, lines 18-22 of Yu, as shown above in modified FIG. 2 of Kazerounian), each of which produces a high voltage from a lower input voltage, would appear to provide no benefits and many detriments to Kazerounian. The circuitry in Kazerounian is specifically designed so that one can select the ***lowest*** V_{OUT} 104 that erases an EEPROM. The selection is performed using the register 106 and a particular process. See the text from col. 8, line 52 to col. 9, line 38 of Kazerounian. Adding another circuit that produces an even higher voltage at V_{OUT} 104 would be counterproductive and may render impossible the careful selection of V_{OUT} 104. For instance, V_{OUT} 104 in such a combined system would now depend on two circuits for producing a high voltage output instead of basically a single

circuit (block 103) in Kazerounian. Furthermore, the Yu circuit does not appear to have an adjustable voltage and does not appear to be able to be controlled by elements (e.g., capacitors 110, the ring oscillator circuit 124, the circuits adjusting V_{REF}, and the comparator 116) in Kazerounian that select a voltage on V_{OUT} 104. Therefore, the combination of Kazerounian and Yu may not provide adjustable V_{OUT}, which is one of the primary reasons Kazerounian was invented.

Third, the combination of Kazerounian and Yu shown in the above figure appears not to work correctly to produce a high voltage on V_{OUT}. For instance, in Kazerounian by itself, the control circuit 107 turns off the transistor 105, which allows V_{OUT} to increase. In the combination circuit shown above, V_{OUT} is grounded by Yu's switching capacitor circuit. However, in order to charge the capacitors in Yu's switching capacitor circuit, V_{OUT} ***has to be grounded***, as the capacitors are charged in parallel and discharged in series. This means that while the capacitors in Yu's switching capacitor circuit are being charged, V_{OUT} 104 is grounded. While V_{OUT} 104 is grounded, the voltage at node 114 is also grounded, which means that the voltage at node 114 does not equal V_{ref}. Ring oscillator circuit 124 (marked incorrectly as 123 in FIG. 2 of Kazerounian) oscillates and the block 103 attempts to produce high voltage on V_{OUT} 104, which is grounded. This means at least that a high amount of power is lost. It is unclear as to what other effect of grounding V_{OUT} 104 while the block 103 attempts to increase voltage will be.

When the capacitors in Yu's switching capacitor circuit are switched into a serial configuration (e.g., the switchers connect A to B), V_{OUT} 104 will now be about three times V_{PP} because each of the three capacitors in Yu's switching capacitor circuit is charged to V_{PP}. For a V_{PP} of 12V (used in Kazerounian), this yields (at least temporarily) a V_{OUT} 104 of 36V, which is the maximum originally made by the voltage multiplier circuit 100 of

Kazerounian (see Kazerounian at col. 9, lines 53-55: "It is noted that in the above-described embodiment, voltage V_{OUT} is a value between 24 and 36 volts, and can be adjusted in 1.2 V steps").

The voltage multiplier circuit 100 of Kazerounian is designed so that $V_{OUT}/4$ is less than or equal to V_{ref}. If $V_{OUT}/4$ is less than V_{ref}, the output lead 119 will be a high voltage and the ring oscillator circuit 124 will operate. If $V_{OUT}/4$ is approximately equal to V_{ref}, the output lead 119 will be a low voltage and the ring oscillator circuit 124 will not operated. It is believed that a condition of having $V_{OUT}/4$ be greater than a certain amount above V_{ref} will cause an undefined condition. Therefore, that the V_{OUT} produced by Yu's switching capacitor circuit will be limited to $V_{ref}*4$. Certainly, using three capacitors in Yu's switching capacitor circuit means that the maximum required voltage by Kazerounian is produced, which would make useless the ring oscillator circuit 124 and the block 103 and the system 128 and capacitors 120, 124, and 126.

On the other hand, if fewer than three capacitors are used in Yu's switching capacitor circuit, the V_{OUT} caused by Yu's switching capacitor circuit should be less than the highest output of the voltage multiplier circuit 100 of Kazerounian. Perhaps it would be possible to use two capacitors in Yu's switching capacitor circuit, which would yield 24V, but again this is the minimum voltage that the voltage multiplier circuit 100 of Kazerounian was originally designed to support. Use of fewer than two capacitors in Yu's switching capacitor circuit would simply yield a single capacitor. Further, the effect of adding Yu's switching capacitor circuit (with capacitors in a series configuration) in parallel with block 103 in Kazerounian is unclear. For instance, if the switching capacitor circuit produces V_{Yu} and block 103 produces V_{Kaz}, what would V_{OUT} be? Would V_{OUT} be the addition of V_{Yu} and V_{Kaz}, the subtraction of V_{Yu} and V_{Kaz}, the highest of V_{Yu} or V_{Kaz}, or some other possibility?

Along these lines, if Yu's switching capacitor circuit produces V_{Yu} and block 103 produces V_{Kaz}, where $V_{Kaz}>V_{Yu}$, what is to prevent the voltage V_{Kaz} from entering Yu'sswitching capacitor circuit and therefore being at least partially unavailable for erasing an EEPROM? As noted above, the V_{Kaz} from the block 103 in Kazerounian has to be higher than the V_{Yu} from Yu's switching capacitor circuit, or else there is no use for the voltage multiplier circuit 100 of Kazerounian.

The Examiner has given no explanation of how adding the switching capacitor circuit in parallel with block 103 in Kazerounian would operate, and therefore a *prima facie* case of obviousness is not shown.

Fourth, Yu's switching capacitor circuit in the combination circuit of Yu's switching capacitor circuit and the voltage multiplier circuit 100 of Kazerounian does not produce a high voltage ***pulse*** as claimed in independent claim 1 ("said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a ***high voltage pulse***"). As described above, when the capacitors of Yu's switching capacitor circuit are charging, the V_{OUT} 104 is grounded. When the capacitors in Yu's switching capacitor circuit are arranged in series, they produce a voltage on V_{OUT} 104. However, block 103 in Kazerounian, now having its output no longer grounded, still has to create whatever voltage is programmed into the voltage multiplier circuit 100 of Kazerounian. This means that Yu's switching capacitor circuit in the combination circuit is not producing a high voltage pulse. Furthermore, independent claim 1 recites the subject matter of "diode chain circuit (22) comprising a diode-chain and pumping capacitors ***for delivering high voltage current***". The block 103 does not appear to deliver a high voltage current.

Fifth, Kazerounian teaches away from a combination of Kazerounian and Yu at, e.g., col. 2, lines 8-19, where Kazerounian states that prior art regulating circuits were too dependent on manufacturing processes. Adding, as the Examiner suggests, a switching capacitor circuit into the system of Kazerounian, where the switching capacitor circuit is not subjected to the voltage regulation of voltage multiplier circuit 100 of Kazerounian, would create the same problem that the invention of Kazerounian was trying to fix.

Finally, the circuit in FIG. 1 of the present disclosure (and as claimed in the claims) is a model of simple functionality for its purpose, whereas the Kazerounian circuit is a complex circuit for another purpose with arrangements for achieving that other purpose.

For at least these reasons, the combination of Kazerounian and Yu is improper and the requirements of a *prima facie* case of obviousness are not met. Independent claim 1 is therefore patentable, as are claims 2-8, which depend from claim 1.

CLAIM 2

The Examiner makes no explicit rejection of claim 2. Claim 2 recites the following: "Capacitive voltage multiplier according to claim 1, characterised in that when high voltage pulse is desired in the switching capacitor circuit (21) the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened and that in stand-by mode (no pulse) the series coupling switches (odd) are open and all other switches (even) are closed in order to charge the pump capacitors from the supply voltage, and that charge sharing will occur with the charge including the load capacitance (103)."

Importantly, claim 2 recites the subject matter "that charge sharing will occur with the charge including the load capacitance (103)." See the following figure from Applicant's specification:

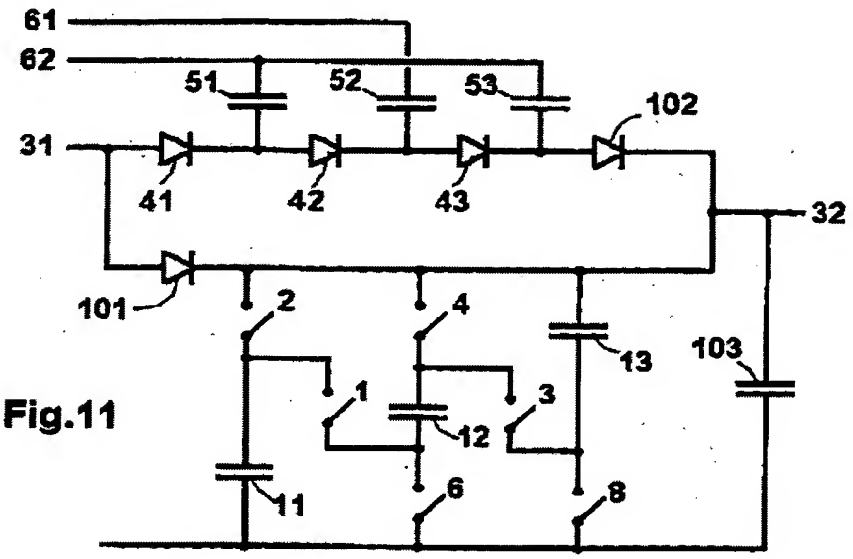


Fig.11

It can be seen that charge sharing between the load capacitance 103 and the capacitors 11-13 can occur, e.g., when the even switches are closed and the odd switches are open. In contraindication, in Yu's switching capacitor circuit shown in FIG. 2 of Yu, the V_{OUT} is grounded when the capacitors C1-C3 are in a parallel (e.g., charging) configuration and charge sharing would not occur between a load capacitance coupled to V_{OUT} and the capacitors C1-C3. When the capacitors C1-C3 of in Yu's switching capacitor circuit are in a series configuration, high voltage is forced onto V_{OUT} and charge sharing would not occur between a load capacitance coupled to V_{OUT} and the capacitors C1-C3.

Kazerounian does not disclose or imply a switching capacitor circuit. Therefore, the combination of Kazerounian and Yu does not disclose the subject matter of claim 2. For at least these reasons, dependent claim 2 is patentable over the combination of Kazerounian and Yu.

CLAIM 3

Dependent claim 3 recites "Capacitive voltage multiplier according to claim 1, characterised in that the switches of the switching capacitor circuit (21) are MEMS switches." The Examiner makes no explicit rejection in the outstanding final Office Action as to where in Kazerounian or Yu this subject matter may be found. Thus, it is unclear as to what is the specific rejection to claim 3. Nonetheless, neither Kazerounian nor Yu discloses use of micromechanical (MEMS) switches. Applicant states the following at page 1, line 32 to page 2, line 2 of Applicant's specification:

> An example of an improved variant of the Marx multiplier called the Mosmarx multiplier was given by P.E.K.Donaldsen: "The Mosmarx voltage multiplier", Electronics & Wireless World, August 1988, pages 748-750. Here metal oxide semiconductors (MOS) switches were used instead of spark gaps. When continuous output is needed high voltage charge is stored in a separate reservoir capacitor, isolated by a serial diode from the output stage, and the switches are operated continuously. The continuous operation prevents the use of micromechanical (MEMS) switches which have a limited lifetime and/or operating frequency.

Applicant further states the following:

> Further, the first voltage multiplier 21 may be of any switching capacitor circuit type suitable for use in voltage multipliers, and the second multiplier 22 can for example be of Crockton-Walton type, but also be of any other type of diode-chain multiplier circuit. Further, instead of semiconductor switches also relays or MEMS (micro electro-mechanical system) switches may be advantageously be used to operate at least the multiplier 21.
>
> In the foregoing a novel method of interconnecting only slightly modified standard voltage multipliers has been presented giving numerous advantages, like decreasing the size of the needed capacitors, and enabling cost effective solutions like the use of MEMS switches, ***hitherto not used in voltage multipliers***, to be employed in future handheld terminals.

Page 7, line 30 to page 8, line 3 (emphasis added) of Applicant's specification. Thus, an exemplary advantage of the disclosed invention is that an embodiment allows the use of MEMS switches.

Kazerounian does not disclose or imply a switching capacitor circuit. Yu does not disclose or imply that MEMS switches may be used for the switchers therein. In fact, FIGS. 3-6 of Yu describe semiconductor swithers.

Because neither Kazerounian nor Yu (nor their combination) discloses that MEMS switches may be used for switches in a switching capacitor circuit and because the Applicant has shown an embodiment able to use MEMS switches when such switches were not used before in such a configuration, Applicant respectfully submits that dependent claim 3 is patentable over Kazerounian.

CLAIM 4

The Examiner made no specific rejection of claim 4. Claim 4 recites "Capacitive voltage multiplier according to claim 1, characterised in that the output of the switching capacitor circuit (21) is activated at the start of a control pulse." Kazerounian does not disclose a switching capacitor circuit. With regard to the combination of Kazerounian and Yu, it is unclear as to how Yu would operate in conjunction with Kazerounian. Certainly, in Kazerounian the control circuit 107 operates to activate the transistor 105 in order to ground V_{OUT}. As stated above, the operation of a combination of Kazerounian and Yu is unclear and basically undefined. Furthermore, the Examiner has made no rejections or comments as to how a combination of Yu and Kazerounian would operate. As there is no disclosure or implication in either Kazerounian or Yu (or their combination) of "the output of the switching capacitor circuit (21) is activated at the start of a control pulse", this claim is patentable over the combination of Kazerounian and Yu.

CLAIM 5

The Examiner made no specific rejection of claim 5. Claim 5 recites "Capacitive voltage multiplier according to claim 4, characterised in that an output of the

switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors."

Kazerounian does not disclose a switching capacitor circuit. As described above with regard to claim 2, charge sharing between the load capacitance 103 and the capacitors 11-13 can occur, e.g., when the even switches are closed and the odd switches are open. In contraindication, in the circuit shown in FIG. 2 of Yu, the Vout is grounded and charge sharing would not occur between a load capacitance coupled to Vout and the capacitors C1-C3. When the capacitors C1-C3 of Yu are in a series configuration, high voltage is forced onto V_{OUT} and charge sharing would not occur between a load capacitance coupled to V_{OUT} and the capacitors C1-C3.

As neither Kazerounian nor Yu disclose the subject matter in claim 5, the combination of Kazerounian and Yu does not disclose the subject matter of claim 5. Therefore claim 5 is patentable over the combination of Kazerounian and Yu.

CLAIM 6

The Examiner made no specific rejection of claim 6. Claim 6 recites "Capacitive voltage multiplier according to claim 4, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level." It is noted that a control pulse is used to enable the switching capacitor circuit (21) and high voltage should be produced during the control pulse duration. See Applicant's specification at pate 7, lines 4-12.

Yu does not disclose a diode chain circuit. Kazerounian has block 103, which the Examiner asserts is a diode chain circuit. Assuming the Examiner assertion is true, the block 103 does not appear to be operated while the V_{OUT} 104 is used to erase an EEPROM. Instead, the block 103 ceases to operate when $V_{OUT}/4 = V_{ref}$, which should occur prior to output of the high voltage used to erase the EEPROM. Kazerounian does not disclose a control pulse or a duration thereof that is used to control high voltage output from a switching capacitor circuit. Kazerounian does disclose a control circuit 107, but the control circuit 107 simply controls a transistor 105, which is used to ground V_{OUT} 104 after erasing the EEPROM. See Kazerounian at col. 6, lines 45-51.

The Examiner has given no indication of how a combination of Yu and Kazerounian would operate. However, if a "control pulse" would be used to operate Yu's switching capacitor circuit in the combination circuit shown above (which Applicant does not admit), it appears that the switches in the Yu circuit would be switched into a series configuration. Regardless, the block 103 of Kazerounian operates only until $V_{OUT}/4 = V_{ref}$, and there is no disclosure or implication that block 103 would be operated during a control pulse duration.

As neither Kazerounian or Yu alone discloses or implies the subject matter of claim 6, the combination of Kazerounian and Yu does not disclose or imply this subject matter. For at least these reasons, claim 6 is patentable over the combination of Kazerounian and Yu.

CLAIM 7

The Examiner made no specific rejection of claim 7. Claim 7 recites "Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) output is through a diode (102) and that no reservoir capacitor is used."

Kazerounian and Yu, alone or in combination, are completely lacking the non-obvious rectifying functions provided by diode 102 (dependent claim 7) (and, e.g., a lack of a reservoir capacitor) in FIG. 1 of Applicant's specification that is important to charge preservation, a concept which is not even discussed in or implied by Kazerounian or Yu or their combination. Therefore, claim 7 presents subject matter not made obvious by the references of record.

CLAIM 8

The Examiner made no specific rejection of claim 8. Dependent claim 8 recites "Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than the incoming supply voltage." As with claim 7, Kazerounian is completely lacking the non-obvious rectifying functions provided by diode 101 (dependent claim 8) in FIG. 1 of Applicant's specification that are important to charge preservation, a concept which is not even discussed in or implied by Kazerounian or Yu or their combination. Therefore, claim 8 present subject matter not made obvious by the references of record.

CONCLUSION

For at least the above reasons, the Applicant/Appellant contends that claims 1-8 are patentable over the combination of Kazerounian and Yu. The Applicant/Appellant respectfully requests the Board reverse the final rejections, and further that the Board rule that the pending claims are patentable over the cited art.

Respectfully submitted:

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11/20/06
Date

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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11/20/2006
Date

(8) CLAIMS APPENDIX

1. Capacitive voltage multiplier for generating voltage pulses, preferably up to 100 V, that are higher than the supply voltage for displays, non-volatile memories and corresponding units especially in small electronic devices, such as handheld telecommunication terminals or corresponding devices,

wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse,

characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier, said diode chain circuit (22) comprising a diode-chain and pumping capacitors for delivering high voltage current.

2. Capacitive voltage multiplier according to claim 1, characterised in that when high voltage pulse is desired in the switching capacitor circuit (21) the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened and that in stand-by mode (no pulse) the series coupling switches (odd) are open and all other switches (even) are closed in order to charge the pump capacitors from the supply voltage, and that charge sharing will occur with the charge including the load capacitance (103).

3. Capacitive voltage multiplier according to claim 1, characterised in that the switches of the switching capacitor circuit (21) are MEMS switches.

4. Capacitive voltage multiplier according to claim 1, characterised in that the output of the switching capacitor circuit (21) is activated at the start of a control pulse.

5. Capacitive voltage multiplier according to claim 4, characterised in that an output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors.

6. Capacitive voltage multiplier according to claim 4, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level.

7. Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) output is through a diode (102) and that no reservoir capacitor is used.

8. Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than the incoming supply voltage.

END OF CLAIMS

(9) EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by Appellant.

(10) RELATED PROCEEDING APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 C.F.R. §41.37.